

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A Circuit for programmable stepless clock shifting comprising:
a splitter, receiving a clock reference and generating two 90°-shifted clock phases, said
splitter comprising a delay circuit receiving said clock reference and supplying a delayed clock;
an adder and a subtractor of said clock reference and said delayed clock, supplying at the output
said two 90°-shifted clock phases, and two squarers for squaring said two 90°-shifted clock
phases, so that said two 90°-shifted clock phases have the same amplitude as one another; and
an interpolator receiving said two 90°-shifted clock phases from said squarers and two
coefficients, and supplying a programmable phase clock, which has a phase shift with respect to
said clock reference that depends only on said two coefficients.

2. (Canceled)

3. (Canceled)

4. (Currently Amended) A Circuit according to claim 21, wherein the delay introduced
by said delay circuit is typically $\Delta = 90^\circ \pm 50\%$, and is

$$\Delta \neq \pi + k\pi, \quad k = \{0, \pm 1, \pm 2, \dots\}$$

5. (Currently Amended) A Circuit according to claim 1, wherein said interpolator

comprises:

a first and second multiplier, respectively receiving one of said two 90°-shifted clock phases and a first and second coefficient; and

an adder receiving the outputs of said first and second multiplier and supplying said programmable phase clock.

6. (Currently Amended) A Circuit according to claim 5, wherein said first and second coefficients have a value of respectively $\sin\Phi$ and $\cos\Phi$, such that the following relationship is performed:

$$\sin(\omega t + \Phi) = \sin(\omega t)\cos\Phi + \cos(\omega t)\sin\Phi$$

where

Φ is said programmable phase of the programmable phase clock;

$\sin(\omega t + \Phi)$ is the frequency of said programmable phase clock; and

$\sin(\omega t)$ and $\cos(\omega t)$ are the frequencies of said two 90°-shifted clock phases.

7. (Currently Amended) A Circuit according to claim 5, wherein said first and second coefficients are selected from a memory table, addressed according to the ~~wanted~~desired programmable phase.

8. (Currently Amended) A Circuit according to claim 6, wherein said first and second coefficient are selected from a memory table, addressed according to the ~~wanted~~desired programmable phase.